ABSTRACT OF THE DISCLOSURE

An apparatus and method for providing early instruction results is disclosed. Early execution logic, comprising an enhanced address generator located in an address generation stage of the microprocessor pipeline, receives input operands and generates early results of instructions reaching the address stage prior to final execution units (in lower pipeline stages) generating final results of the instruction for updating an architected register file. The early execution logic is configured to execute only a subset of the instructions in the microprocessor instruction set. The early results are invalid if the instruction is not in the subset. An early register file corresponding to the architected register file stores the early results and also provides the early results to the early execution logic as input operands. The generated early results are invalid if any input operands are invalid. Early status flags accumulated from the early results enable selective early execution of conditional instructions.